

A GENERALISED INTEGRATOR

**A Thesis Submitted In Partial
Fulfilment of the Requirement
For the Degree of Master of Technology**

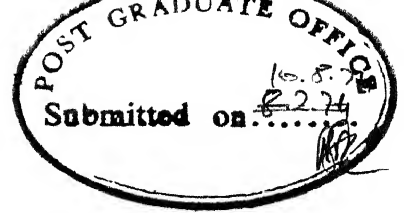
by

A. S. RANADE.

to the

**DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY, KANPUR.**

August 1974.



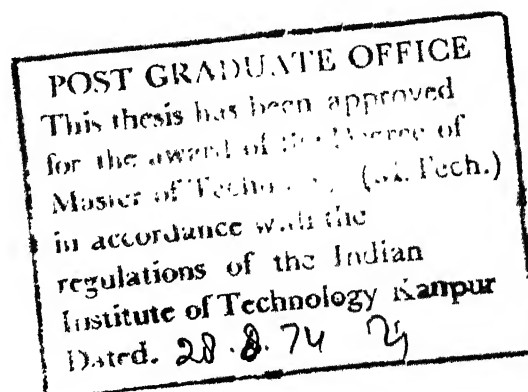
CERTIFICATE

This is to certify that the thesis entitled 'A Generalised Integrator' is a bonafide record of the work done under my supervision and that it has not been submitted elsewhere for a degree.

P. Ramakrishnarao.

Kanpur,
August 1974.

Dr. P.R.K. Rao
Department of Electrical Engineering
Indian Institute of Technology, Kanpur.



I.I.T. KANPUR
CENTRAL LIBRARY
Acc. No. A 30232

13 SEP 1974



EE-1974-M-RAN-GEN

ACKNOWLEDGEMENT

I wish to acknowledge my deep sense of gratitude to Dr. P.R.K. Rao for his guidance and encouragement.

I would like to express my sincere thanks to all my friends, particularly Mr. Ashok Bhattacharya, who gave valuable suggestions at crucial moments.

Thanks are also due to Mr. S.S. Pethkar for the neat job of typing and to Mr. B.N. Srivastava who has drawn the figures.

A. S. Ranade

CONTENTS

CHAPTER	TITLE	Page No.
1	INTRODUCTION	1
2	REALIZATION OF THE GENERALISED INTEGRATOR	2
3	CIRCUIT DIAGRAMS	7
4	INTEGRATOR EQUATIONS	18
5	APPLICATIONS	24
6	MODIFIED VERSION OF THE GENERALISED INTEGRATOR	30
7	CONCLUDING REMARKS	39
	REFERENCES	42

CHAPTER 1

INTRODUCTION

The conventional analog computer is limited in capability in that it can integrate its input signals only with respect to the independent variable that is time. The generalised integrator, which is discussed in the sections that follow is capable of integrating a function with respect to yet another function of time. The unit is a hybrid analogue-digital device and uses delta modulation techniques. It is particularly useful in function generation and can handle signal frequencies upto 100 c/s within 1% error. [Theoretical and practical work on this unit was earlier reported in literature by Paul and Gatland (Ref.1)].

[The scheme of this report is as follows. In Chapter 2, the realisation is discussed. Chapter 3 gives circuit details. Analysis is done in Chapter 4. Chapter 5 is devoted to applications. In Chapter 6 the modified version of the integrator is discussed and concluding remarks are put in Chapter 7.]

CHAPTER 2

REALIZATION OF THE GENERALISED INTEGRATOR

2.1. Basic System:

Let $y(t)$ and $x(t)$ be the two separate functions of time. The objective is to generate the function $\int_0^t y(t) dx(t)$. A method of realizing the above integral is as follows.

$$\int y(t) dx(t) = \int y(t) \frac{dx(t)}{dt} \cdot dt \quad (1)$$

The identity (1) decides the units that will have to be employed to get the desired result.

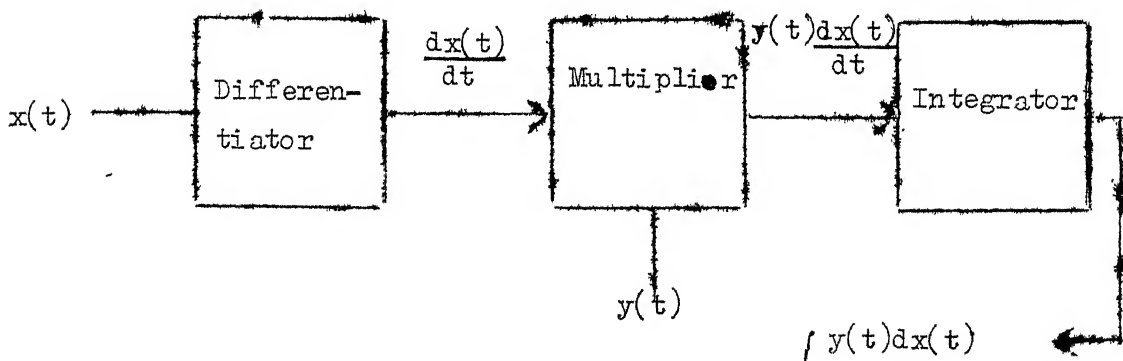
It is necessary to have a block that will differentiate the function $x(t)$ with respect to time.

A multiplier will be needed to obtain the product $y(t) \cdot \frac{dx(t)}{dt}$.

And finally a conventional integrator will have to be used which will integrate the above product with respect to time.

Thus the block diagram shown in Fig.1 is appropriate.

Fig. 1



The system, therefore, has three main units. These are described below.

2.2. Differentiator:

A differentiator which is based on active R-C networks suffers from the disadvantage that the gain increases with the increase in frequency and hence the immunity to high frequency noise is low. Hence a different method is employed to effect differentiation.

The method that is discussed below is due to Paul and Gatland. See reference 1.

The variable $x(t)$ is sampled and quantised in such a way that it is measured in discrete amplitude steps $\delta x = \pm q$ at discrete time intervals separated by $\delta t = T_c$, where $1/T_c$ is the sampling rate and q is the constant quantisation level. The variable $x(t)$ should, therefore, vary in such a way that its maximum rate of change is less than one quantum in time T_c . In other words,

$$\frac{q}{T_c} \geq \left(\frac{dx(t)}{dt} \right)_{\max} \quad (2)$$

If the above equation is satisfied δx may be expressed in the form

$$\delta x = q u_x$$

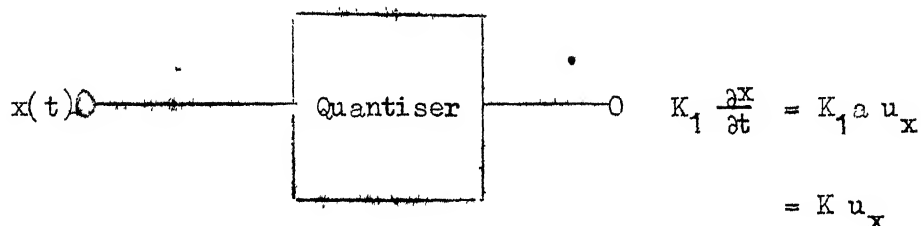
where u_x is a train of impulses occurring at discrete time intervals T_c , having a unit magnitude and a positive or negative sign according to the time rate of change.

Thus

$$\frac{\partial x}{\partial t} = \left(\frac{q}{T_c} \right) u_x = a u_x \quad (3)$$

where $a = \frac{q}{T_c}$.

The output of the actual quantiser, as shown in Fig. 2, will contain a scaling constant to suit circuit conditions.



where $K = a K_1$

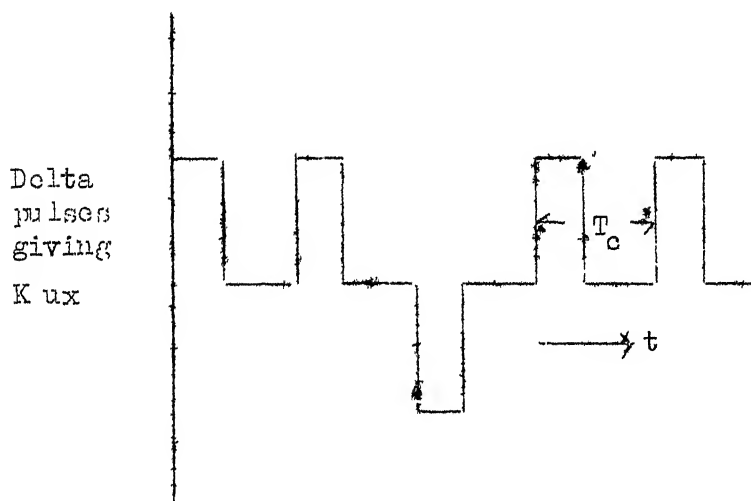
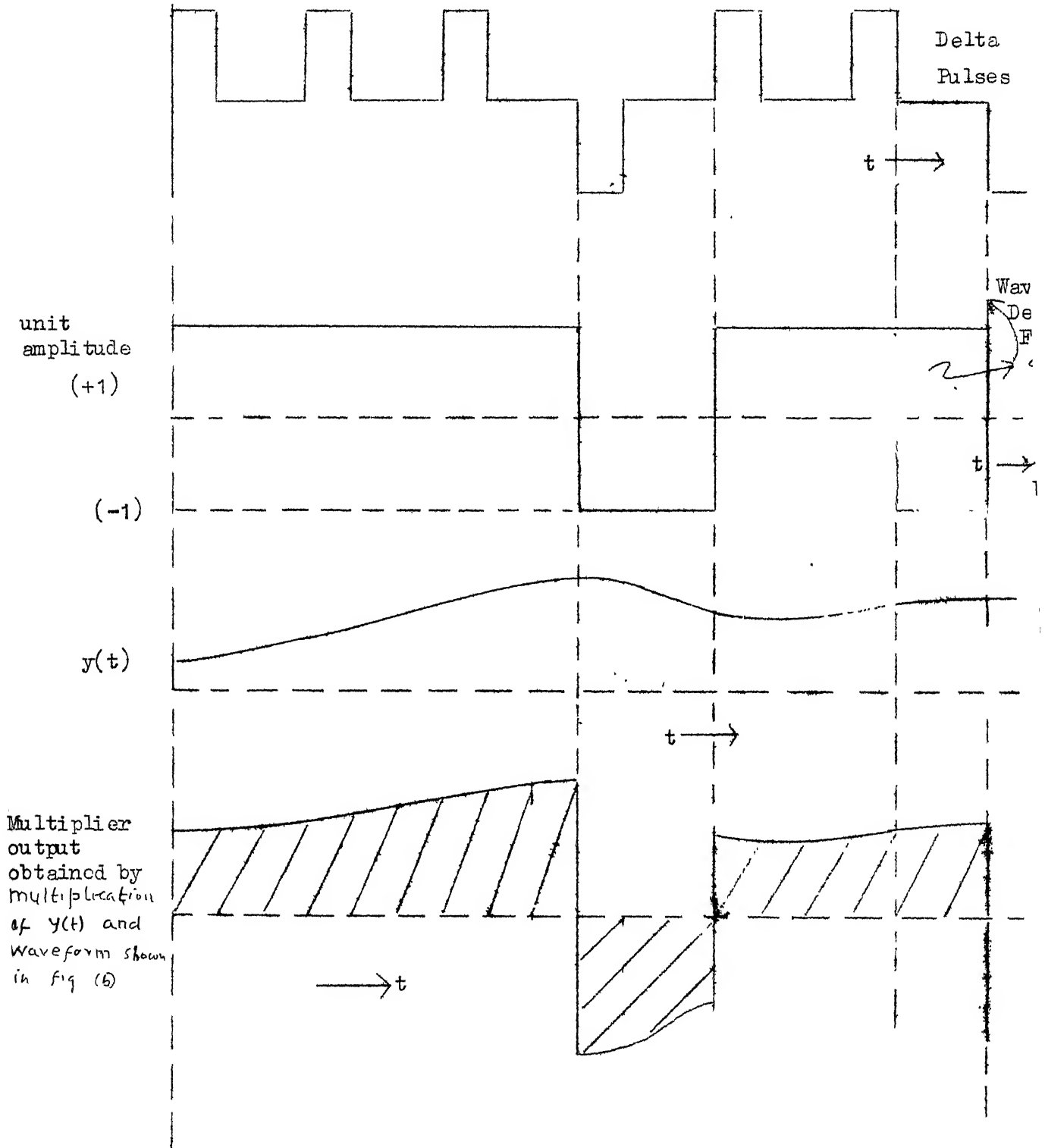


Fig. 2

2.3. Multiplier and the associated integrator

Multiplication of the analog signal $y(t)$ and the signal $K u_x$ (which is represented by the edges of the delta pulses shown in Fig.2) is done in the following way. Positive values of the analog signal are transmitted to the output as long as the sign of the delta pulses remains

Fig. 3

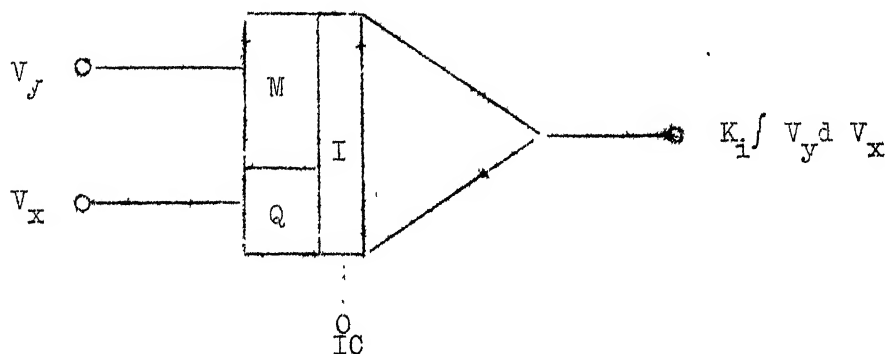


positive. As soon as the next delta pulse changes sign negative values of the analog signal $y(t)$ are transmitted to the output and this is continued until the next delta pulse changes sign again where upon again positive values of the signal $y(t)$ are transmitted to the output and so on. This is illustrated in Fig. 3.

Integrator: This is a conventional analogue integrator the circuit of which is described in Section 3.4. There is also a provision for applying the initial condition voltage to this integrator. The circuit details for this are given in Section 3.5.

2.4. Symbol for the generalised integrator

The three main units of the integrator can be incorporated in a symbolic notation so that the applications where various such integrators are used can be easily illustrated by the diagram using the symbolic notation.



In the above symbol Q stands for quantiser; M for multiplier and I for the integrator associated with the multiplier.

IC is initial-condition voltage

K_i is integrator scale factor.

CHAPTER 3

CIRCUIT DIAGRAMS

3.1. Quantiser : This unit is based on the block diagram shown in Fig. 4

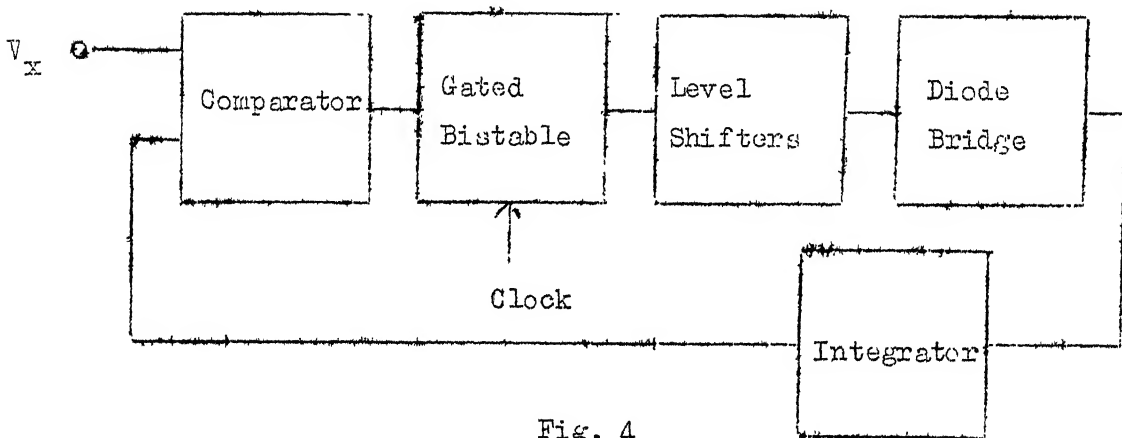


Fig. 4

This is essentially a feedback control system in which the correspondence between the input V_x and the integrator output is maintained. Consider a situation when the integrator output voltage is greater than the input voltage V_x . Under this condition the outputs of the comparator, the bistable and the level shifters are at one of the two possible levels. The level of the final level-shifter is such that it causes, via diode bridge, the output of the integrator to linearly decrease, thus approaching the value of V_x . As soon as the output crosses the value of V_x the comparator output will change. The flip-flop will also change state at the next clock edge. The states of the succeeding stages will change so that the integrator output will start increasing linearly and will

approach V_x again.

In other words the output will be a triangular approximation of the input waveform. The rate at which the integrator output increases or decreases corresponds to the term q/T_c of equation (3).

And the output pulses of the flip-flop and level shifters represent, the term dx/dt . It is important to note that the output waveform (V_j) of the level shifters, shown in figure 5, as also the output waveform of the flip-flop, corresponds to the waveform shown in fig. 3(b). And since this is the waveform required for multiplication of $y(t)$ and the term dx/dt , it is not necessary to generate the pulses shown in fig. 3(a).

WAVEFORMS IN THE QUANTISER

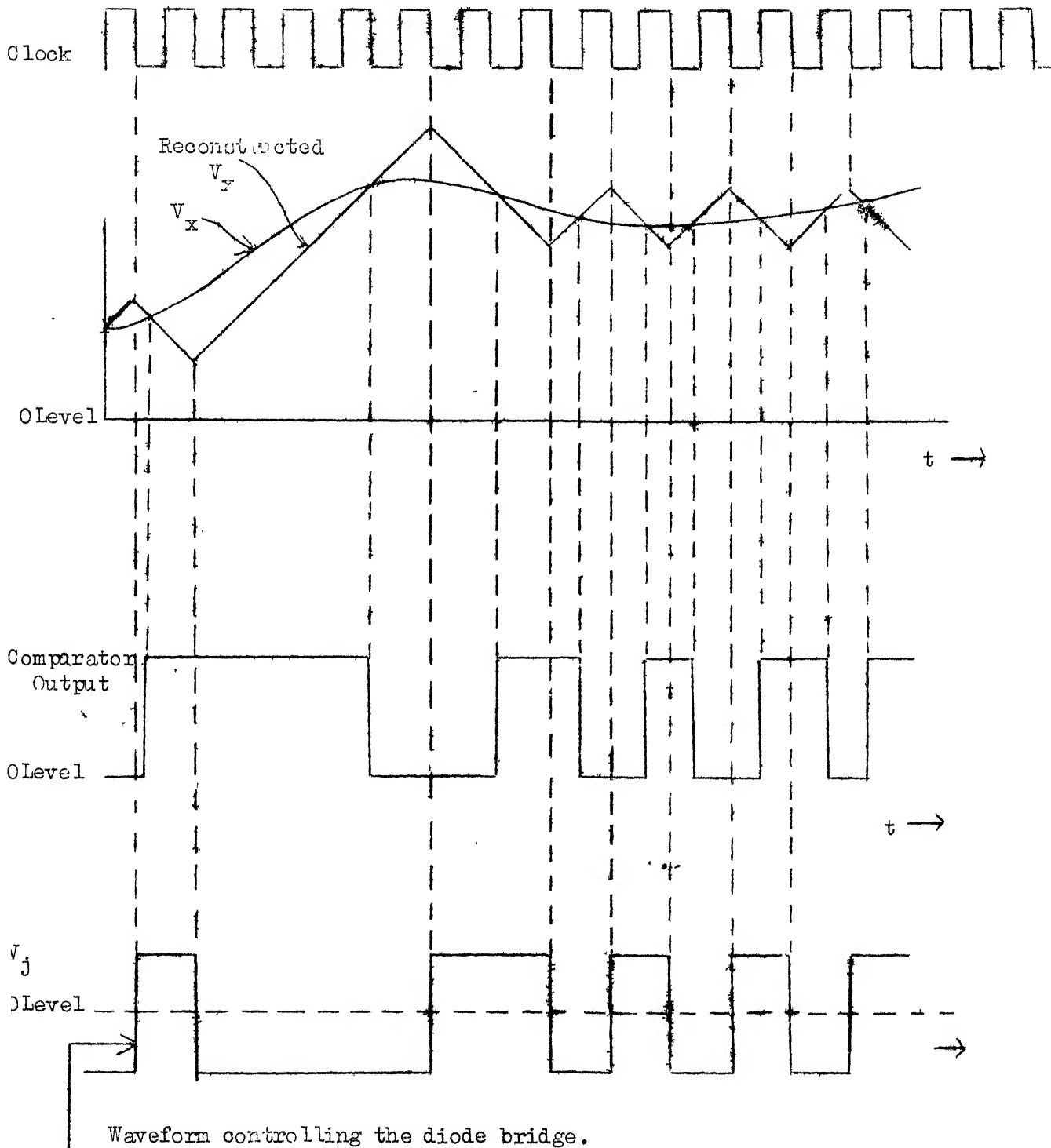


Fig. 5

3.2. Circuit details in the quantiser:-

The actual circuitry used is shown below.

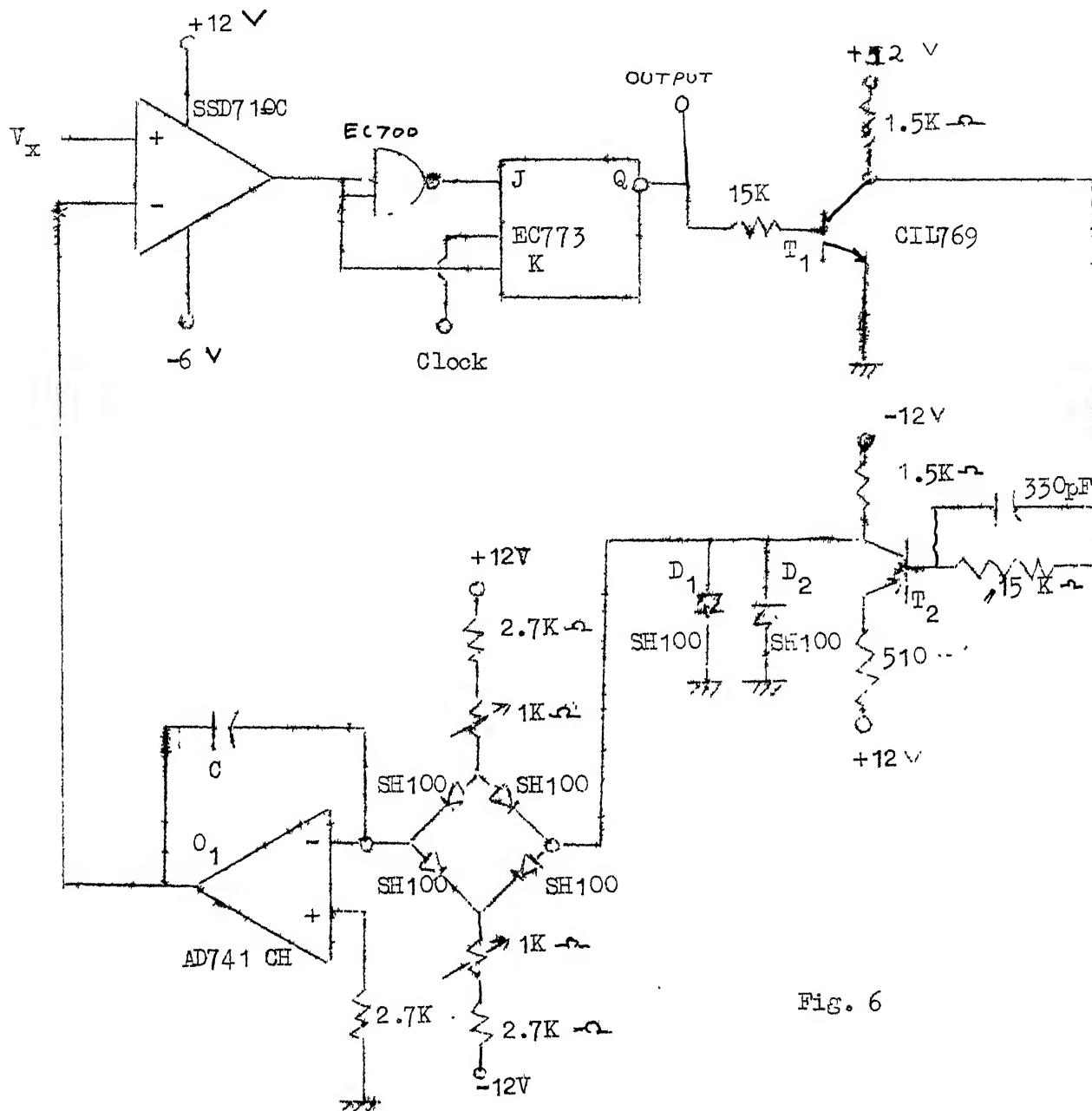


Fig. 6

For reasons explained in section 4.2 the clock frequency is chosen to be 100 Kc/s. And the fastest rate, at which the comparator output will have to change, will be close to this. The SSD 710C Comparator that is used easily accommodates this rate. The flip-flop EC773 is used in the D-mode and thus represents the gated bistable of the block diagram shown in fig. 4. The transistors T_1 and T_2 do the job of level shifting. The diodes D_1 and D_2 clamp the levels to $\pm .6$ volts which are appropriate for controlling the diode bridge. The Op-Amp 741 is used in the usual integrating mode. The term q/T_c of the equation (3) corresponds to I/C in the above circuit, where C is the integrating capacitor ($1 \mu F$) and I is the current switched by the diode bridge. By keeping the circuit in the open-loop mode (i.e. grounding the negative terminal of the comparator and breaking the feedback connection) the positive and negative slopes were adjusted to be equal by using the 1K trimpots shown. The slope was adjusted to be 3125 Volts/second. The factors deciding the choice of the slope are discussed in the section 4.1.

Since the comparator used (SSD 710C) can not handle an input signals of more than ± 5 Volts, this is the maximum amplitude of V_x that can be fed to the quantiser.

3.3. Circuit for the clock

The usual astable multivibrator is used for generating the clock pulses.

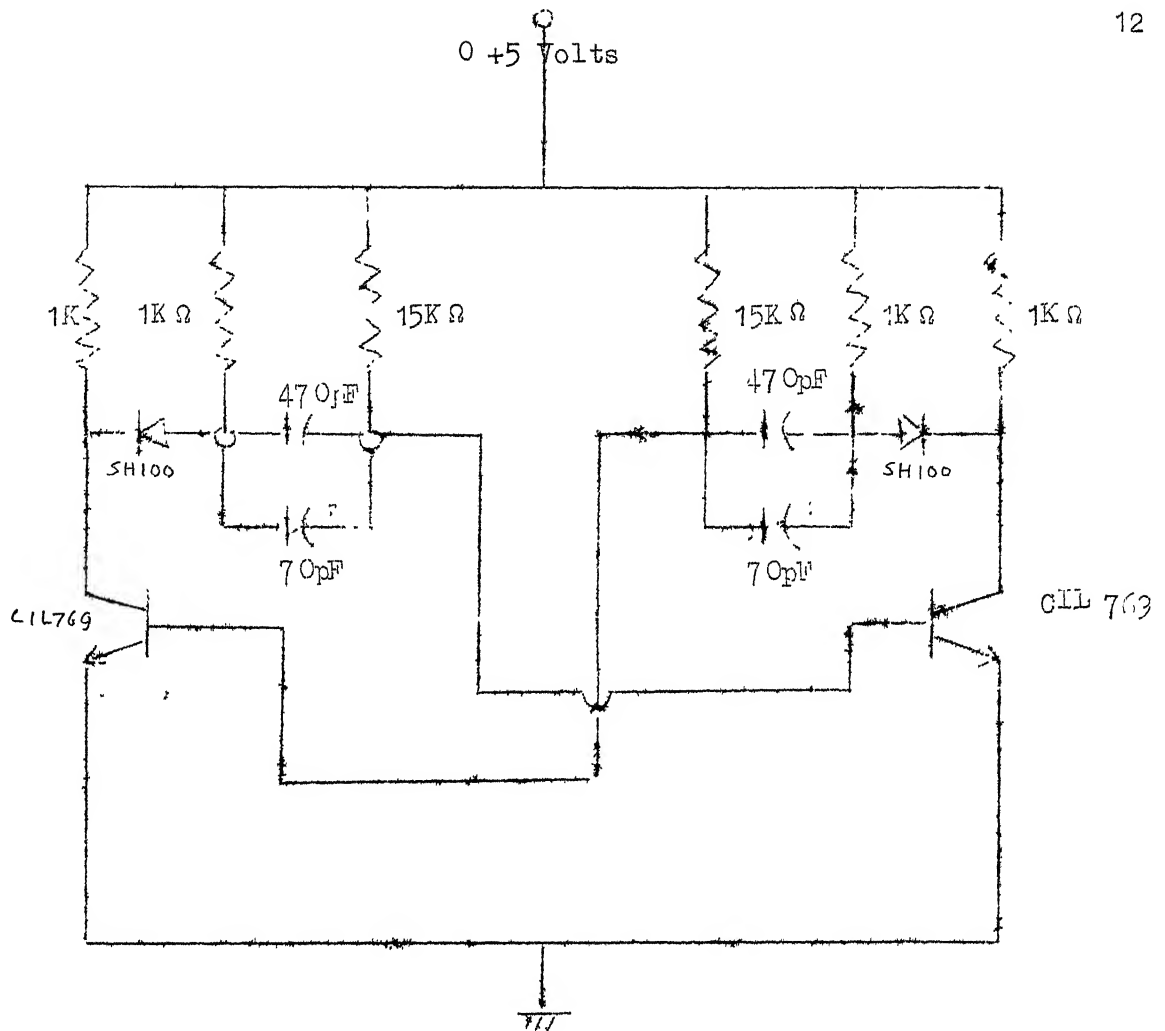
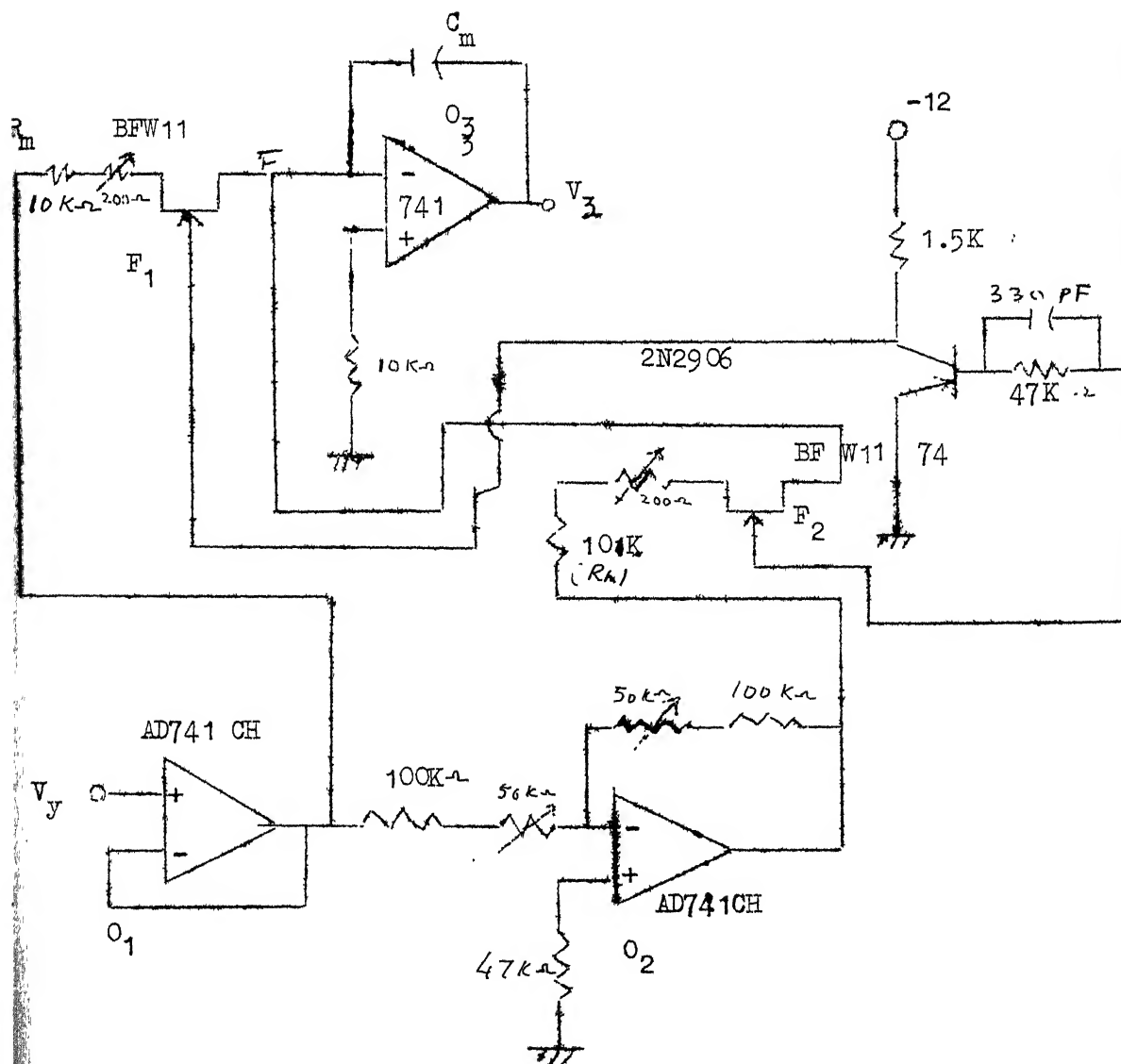


Fig. 7

The levels for the clock are chosen such that they are compatible with the TTL flip-flop that is used in conjunction with the clock.

3.4. Circuit diagram for the multiplier and the associated integrator

The circuit shown in Fig. 8 accomplishes the function of multiplication as well as the integration. The transistors T_1 , T_2 , T_3 and T_4 act as level shifters to obtain the proper levels for operating the



FETS, F_1 and F_2 . The source point of both the FETS is connected to the inverting terminal of the integrating OP-AMP O_3 . Hence this point is virtual earth. Thus when T_4 is in saturation the gate-source voltage of F_1 is -3 volts and F_1 is ON. When T_4 is off gate source voltage is -12 volts and the FET F_1 is OFF. Similar argument applies for T_3 and F_2 .

The Op-AMP O_1 acts as a buffer for the input voltage V_y . The OP-AMP O_2 is connected to invert V_y . When F_1 is ON the current of the value V_y/R_m is forced into the integrator O_3 . And when F_2 is ON the current of the value $-V_y/R_m$ is switched into the integrator. In this connection it is important to note that the level shifting inverters are appropriate in number so that $+V_y/R_m$ current is switched into the integrator when the waveform V_j of fig. 5, which represents $\frac{dx}{dt}$, is positive and the current $-V_y/R_m$ is switched when V_j is -ve.

In fig. 8 the OP-AMP O_3 , used as integrator, is shown connected such that it is permanently in the operate mode. However, as was mentioned in section 2.3, it is necessary to make provisions for applying the initial condition. This is discussed in the following section.

3.5. The IC and COMPUTE modes of the integrator.

These two modes are illustrated in the fig. 9.

The integrator is in the compute mode when the switch S_1 is on C and S_2 is open. And it is in the initial condition mode when the

switch S_1 is on I.C. and S_2 is closed.

In many cases it is necessary to apply the initial condition and to compute alternately. Repetitive operation is then required. In analog computers the initial condition is provided at the time $t = 0$, since the integration is with respect to time. But in many applications of the generalised integrator it is necessary to apply the initial condition at $V_x = 0$. The system shown in Fig. 10 performs this operation.

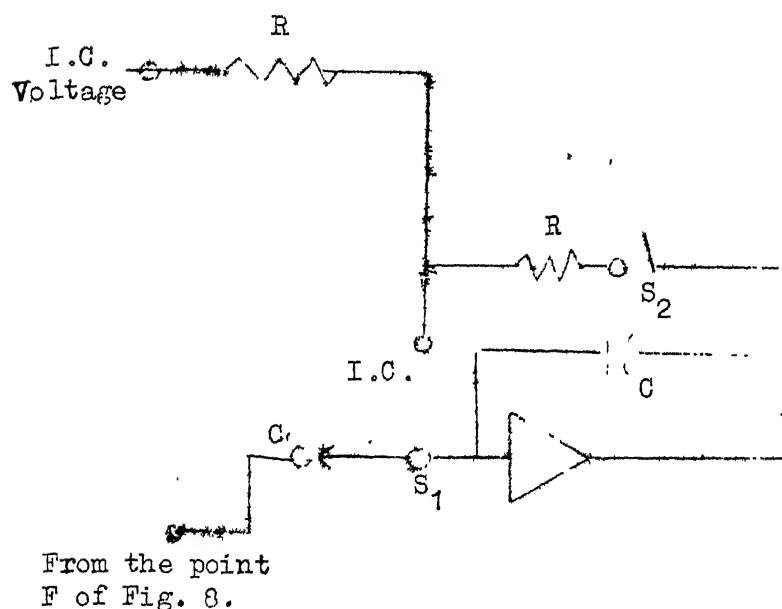


Fig. 9

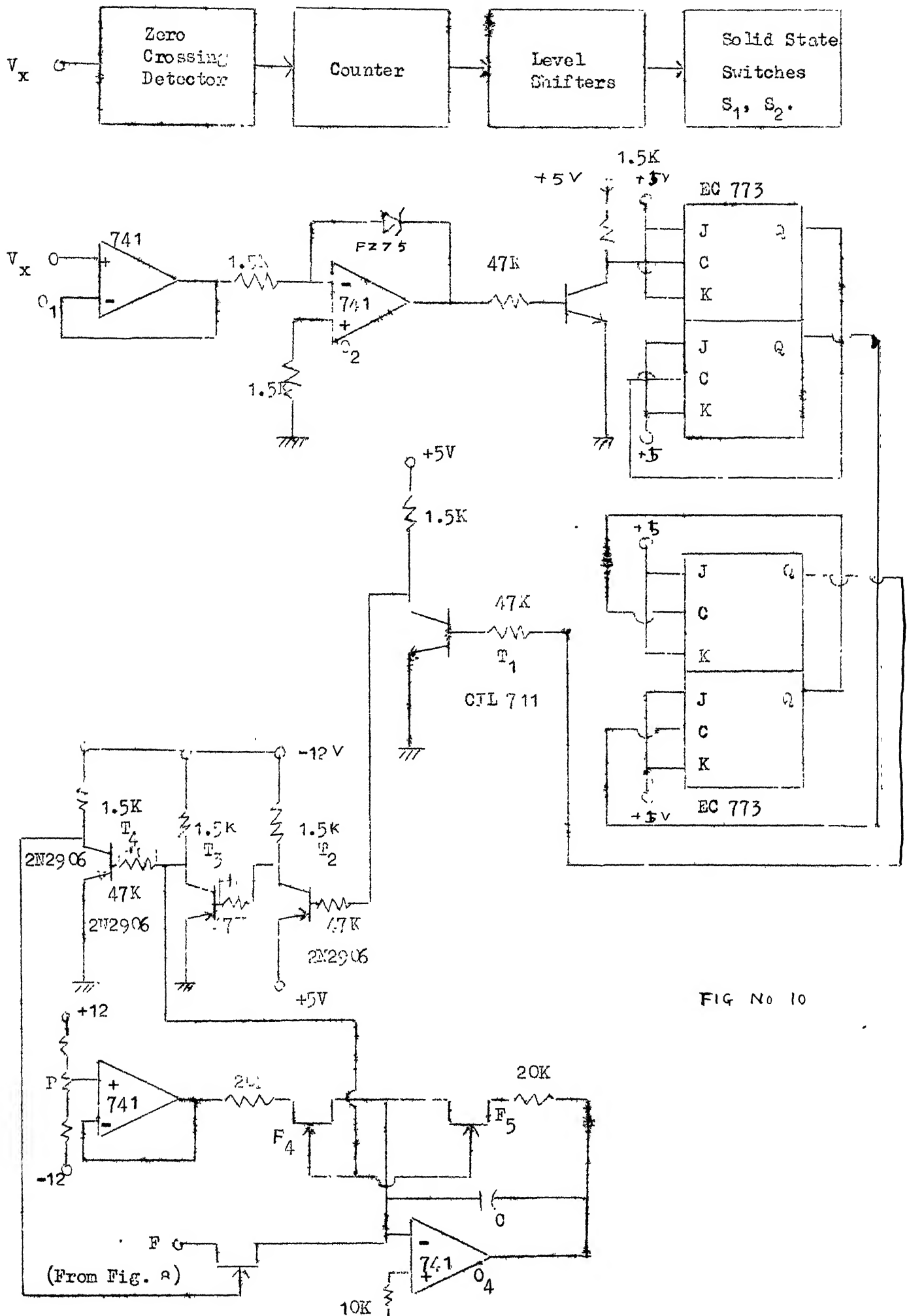


FIG No 10

The OP-AMP O_1 is used as a buffer for the signal V_x . The OP-AMP O_2 is used as a zero crossing detector. The two I.C. chip-flip flops (EC773) give a count of 16. The transistors T_1 , T_2 , T_3 and T_4 are used for operating the FETS F_3 , F_4 and F_5 . The gates of F_4 and F_5 are connected together and therefore they will both be OFF for compute period and be ON for initial condition period. The initial condition voltage can be set by the potentiometer 'P' of fig. 10.

It is to be noted that the compute time corresponds to 8 cycles and the time for setting of the initial condition also corresponds to 8 cycles.

As discussed in Section 5.2 the maximum frequency of the signal is limited to 100 c/s. Thus 8 cycles will have a minimum time of 80 m secs. Now for the initial condition mode the effective time constant is (if $C = .15 \mu F$) 1.5 m secs. Thus 80 m secs is sufficient for the capacitor to acquire new required voltage at the end of initial condition time.

CHAPTER 4

INTEGRATOR EQUATIONS

4.1. The Scaling Factor:

The purpose of analysis that is done in this section is to obtain an expression for the integrator constant (mentioned in the Section 2.4) in terms of the time constants associated with the quantiser integrator and the integrator used in the multiplier.

With reference to the quantiser unit (Fig.6), the output of the integrator O_1 is given by

$$-V_x = \int \frac{I}{C} \cdot \frac{V_j}{|V_j|} dt \quad (4)$$

where I is the current switched by the diode bridge and C is the integrating capacitor that is shown in Fig. 6. $\frac{V_j}{|V_j|}$ is the switching function having a unit magnitude and a sign corresponding to the sign of the waveform V_j shown in Fig. 5.

Equation (4) can be rewritten as

$$\begin{aligned} \frac{dV_x}{dt} &= - \frac{I}{C} \frac{V_j}{|V_j|} \\ \text{or} \quad \frac{V_j}{|V_j|} &= - \frac{C}{I} \frac{dV_x}{dt} \end{aligned} \quad (5)$$

And with reference to the circuit of the multiplier and the associated integrator (Fig.8), the voltage output V_z may be expressed as

$$V_z = - \frac{1}{T_m} \int \frac{V_j}{|V_j|} V_y dt \quad (6)$$

From the equations (5) and (6),

$$V_z = \frac{C}{I \cdot T_m} \int V_y \cdot \frac{dV_x}{dt} \cdot dt$$

or
$$V_z = \frac{C}{I \cdot T_m} \int V_y dV_x$$

or
$$V_z = K_i \int V_y dV_x, \quad (7)$$

if
$$K_i = \frac{C}{I \cdot T_m} \quad (8)$$

K_i is called the integrating factor and can be changed by changing any of the three factors i.e. I , C and T_m . Thus scaling can be done at will by varying the above factors.

It should be noted, however, that the ratio I/C has also to be adjusted such that the equation (2) is satisfied.

4.2. Choice of clock frequency

The sampling frequency must be chosen so that the modulation signal $K u_x$, representing a voltage dV_x/dt , contains all the frequency components of the latter having an amplitude exceeding the maximum tolerable error, expressed as a percentage of full scale amplitude. The signal $K u_x$ may be expressed as

$$K u_x = \sum_{n=1}^{\infty} a_n \sin\left(\frac{\omega_c t}{n} + \phi_n\right) + \sum_{m=2}^{\infty} b_m \sin(m \omega_c t + \phi_m)$$

where ω_c is the angular frequency of the clock sampler, a_n and b_m are constants and ϕ_n and ϕ_m are phase shifts. The first term in the above equation contains the signal and the second term represents the noise generated in the delta modulation process. Since the carrier can not accommodate any signal of frequency exceeding one half of its own, i.e. $\omega_c/2$, the latter is therefore the maximum possible significant signal frequency.

The required sampling frequency depends on the frequency content of the analog signal. The most severe case with which the quantiser must contend is that of an input V_x which is a triangular wave with a rate of change equal to that of the maximum possible rate of increase of voltage of the quantiser,

i.e. I/C . This waveform is shown in Fig. 10,* together with its derivative dV_x/dt .

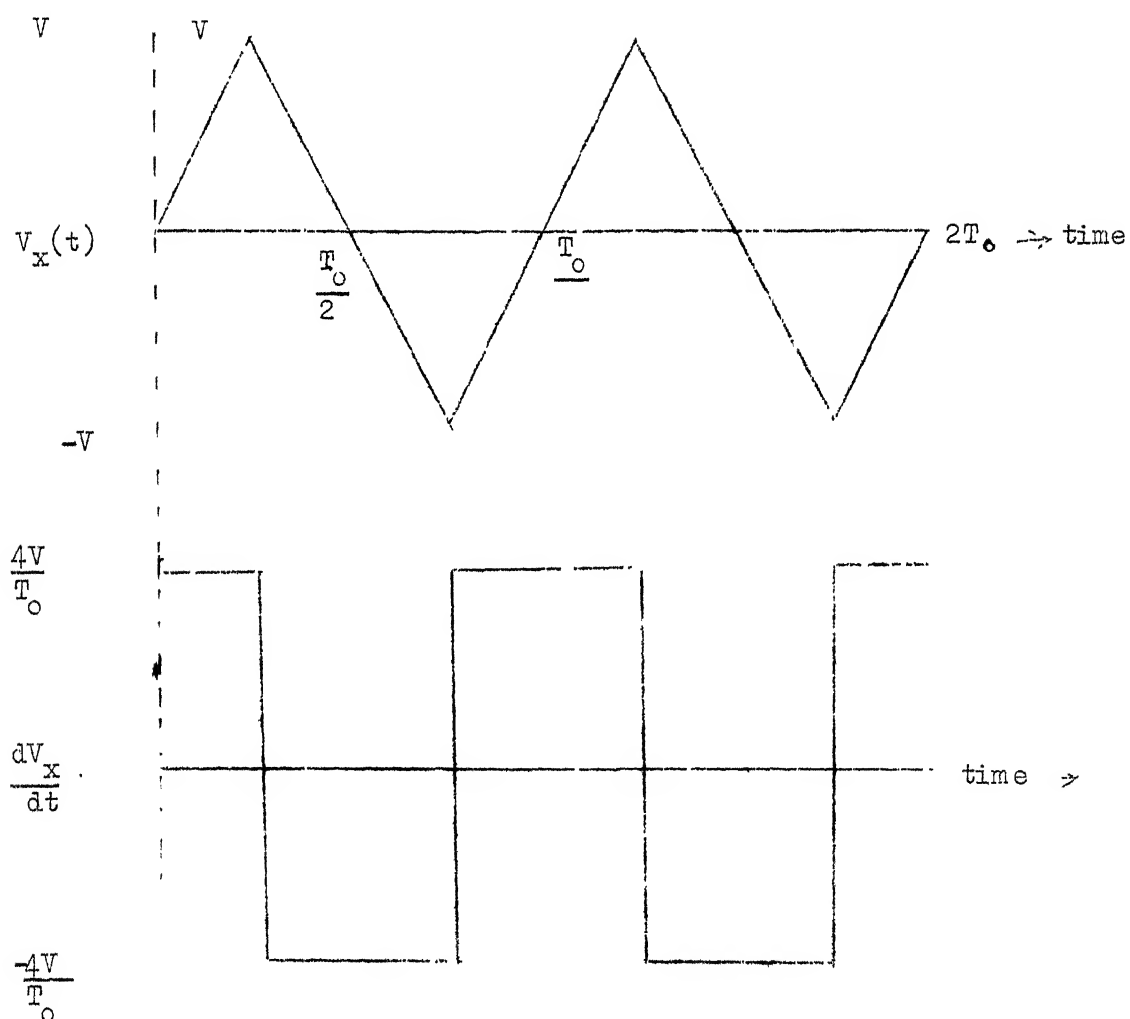


Fig. (10)*

The dV_x/dt waveform will, to a high degree of approximation, be identical in form to that of the switching waveform V_j .

The Fourier series expansion of the function dV_x/dt , but normalised to have a maximum amplitude V by multiplying by the scale factor $T_0/4$, is

$$\frac{T_0}{4} \frac{dV_x}{dt} = \frac{4V}{\pi} \sum_{n=1}^{\infty} (-1)^{n-1} \frac{1}{2n-1} \cos(2n-1)\omega_0 t$$

where $\omega_0 = \frac{2\pi}{T_0}$ and n is an integer.

Now the highest significant frequency in the waveform, represented by the above equation, is defined as that frequency component which has the amplitude equal to the quantisation level q .

Thus if r th harmonic is considered to be the highest significant frequency, its amplitude is given by

$$\frac{4V}{r\pi} = q$$

$$\text{or} \quad \frac{4V}{r\pi} = NV$$

where N is the discrimination accuracy defined as $N = q/V$.

The clock frequency must, therefore, be twice the frequency corresponding to the r th harmonic of ω_0 i.e.

$$\omega_c \geq \frac{8\omega_0}{N\pi} \quad (1)*$$

As stated, $\frac{4V}{T_0}$ represents the maximum possible rate of change of the quantiser output voltage i.e. I/C .

Thus, if w_m is the maximum angular frequency that can be accommodated when $V_x = V \sin w_m t$,

$$w_m V = \frac{4V}{T_0}$$

or
$$w_m V = \frac{2w_0 V}{\pi} \quad (2)^*$$

From equation (1)* and (2)*

$$w_0 \geq \frac{4w_m}{N}.$$

Thus if $N = 10^{-3}$, i.e. .1% accuracy and if $f_0 = 100$ kc/s,

where $w_0 = 2\pi f_0$,

$$f_m = 25 \text{ c/s.}$$

However f_m can be increased at the expense of accuracy. If

now $N = 10^{-2}$

$$f_m = 250 \text{ c/s.}$$

CHAPTER 5

APPLICATIONS

5.1. Generation of functions by integration techniques

Generation of functions of variables which are themselves functions of time is an important application of this integrator. In conventional analog computers such functions are generated by methods which are expensive and are difficult to set up. Some examples of generation of functions by the generalised integrator are described in the sections that follow.

5.2. Generation of exponential function $m e^{kx}$:

The function $y(t) = m e^{kx(t)}$ can be generated in the integrator by the following method.

The above equation can be rewritten using the computer voltage variables. That is

$$V_y = m e^{KV_x} \quad (5.1)$$

where V_y is the computer voltage that represents the analog variable $y(t)$ and V_x is the voltage that represents the analog variable $x(t)$.

From the equation (5.1)

$$\frac{dV_y}{dV_x} = Km e^{KV_x}$$

or
$$\frac{dV_y}{dV_x} = KV_y$$

and hence

$$V_y = K \int V_x \, dV_x$$

with initial condition for $V_y = m$ when $V_x = 0$. Thus if $K = K_i$, where K_i is given by equation (8), the following arrangement can be used.

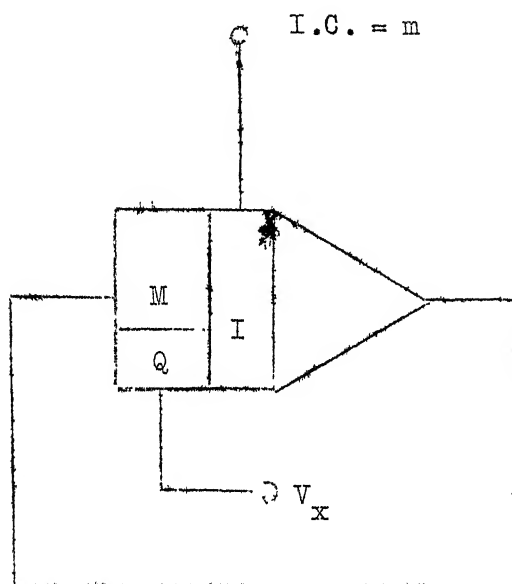


Fig. 11

As an example, $V_x = V \sin \omega t$. Then

$$V_y = m e^{\frac{K_i V}{I} \sin \omega t} \quad (5.2)$$

Now
$$K_i = \frac{C}{I \cdot T_m} \quad (\text{Volts})^{-1}$$

I/C is the rate at which the voltage output of the integrator (used in the quantiser) is changing. This is chosen in the following way.

I/C must be greater than the maximum rate at which V_x is changing. And this rate is wV .

$$\text{If } w = 2\pi \cdot 100 \text{ c/s,}$$

$$\text{then } wV = 2\pi \cdot 100 \cdot 4 = 800 \text{ Volts/sec.,}$$

$$\text{for } V = 4 \text{ Volts.}$$

So, for the circuit to work, I/C must be greater than 800 V/sec. It is mentioned in Section 3.2 that I/C is adjusted to be 3125 Volts/sec. As this is more than wV (800 Volts/sec.), the operation will be satisfactory.

Actually the rate I/C can be increased to accommodate larger signal frequencies. However this will reduce the value K_i and hence the output voltage will be attenuated more. (See equation 5.2).

The amplitude can also be controlled by the factor T_m which is the time constant associated with the integrator used in the multiplier unit. The reduction in T_m will increase the amplitude.

Now T_m is $R_m \cdot C_m$ (See fig. 8). As can be seen from the fig. 8, R_m controls the current fed into the OP-AMP O_3 . Hence this can not be arbitrarily reduced. Also R_m has to be large enough to swamp the resistances of the FETs so that a definite accuracy is obtained. The reduction in the value of C_m will also cause an increase in the amplitude of the output voltage. Still, a higher value of C_m will mean better filtering of the switching components.

Thus, with $I/C = 3125 \text{ Volts/sec.}$

$$R_m = 10 \text{ K}\Omega$$

$$C_m = .15 \text{ }\mu\text{F.}$$

$$K_i = \frac{1}{4.687} \text{ (Volts)}^{-1}$$

And if $V = 4$ Volts, the amplitude of V_y is given by

$$V_{ym} = m e^{4/4.687}$$

$$V_{ym} = 2.343 \times m$$

If m , which is the initial condition voltage, is 2 volts, then

$$V_{ym} = 4.686 \text{ Volts.}$$

5.3. Generation of Sine and Cosine Functions

The function $y(t) = P \sin m x(t)$ and $y(t) = P \cos m x(t)$ can be generated as shown below.

Let, as before, V_y and V_x be the computer voltage variables and consider the following circuit

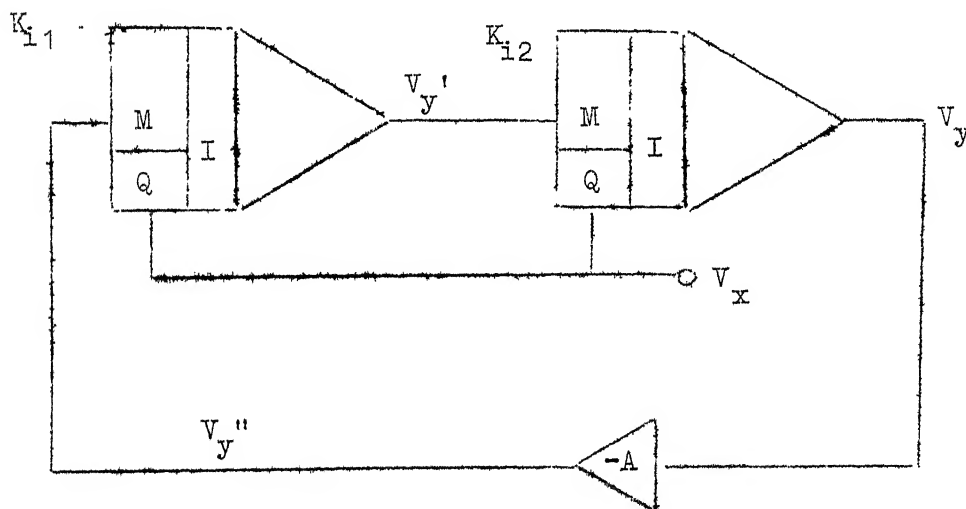


Fig. 12

K_{i1} , K_{i2} are the integrator constants as defined by the equation (8).

Now, V_y' can be written as

$$V_y' = K_{i1} \int V_y'' dV_x.$$

But
$$V_y'' = -\Lambda V_y.$$

Therefore,

$$V_y' = -\Lambda K_{i1} \int V_y dV_x$$

Also V_y is given by

$$V_y = K_{i2} \int V_y' dV_x$$

or
$$V_y = -\Lambda K_{i1} K_{i2} \int \left(\int V_y dV_x \right) dV_x.$$

Hence

$$\frac{dV_y}{dV_x} = -\Lambda K_{i1} K_{i2} \int V_y dV_x$$

or
$$\frac{d^2 V_y}{dV_x^2} = -\Lambda K_{i1} K_{i2} V_y \quad (5.3)$$

And the solution to the equation (5.3) is

$$V_y = P \cos \sqrt{\Lambda K_{i1} K_{i2}} V_x \quad (5.4)$$

with the initial condition,

$$V_y = P \text{ at } V_x = 0.$$

Also
$$\frac{dV_y}{dV_x} = -P \sqrt{\Lambda K_{i1} K_{i2}} \sin \sqrt{\Lambda K_{i1} K_{i2}} V_x,$$

With the initial condition

$$\frac{dV_y}{dV_x} = 0, \text{ at } V_x = 0.$$

As an example consider a case when V_x is a triangular wave such that,

$$V_x = Kt \text{ for } 0 < t < T/2$$

where $T/2$ is half the period of the triangular wave.

Then, for the time between 0 and $T/2$,

$$V_y = P \cos \sqrt{A K_{i1} K_{i2}} Kt$$

$$\text{Then } w = \sqrt{A K_{i1} K_{i2}} \cdot K.$$

Now if $K = 400$ Volts/sec.

And $A = 1, K_{i1} = K_{i2} = 1/4.687$

$$w = 400/4.687 \text{ r/sec.}$$

or $f = 13.6 \text{ c/s.}$

CHAPTER 6

MODIFIED VERSION OF THE GENERALISED INTEGRATOR

6.1. Modified Quantiser:

The quantiser unit can be modified so that the delta pulses represent the signal V_x itself rather than its time derivative. The modified block diagram of the quantiser unit is shown in Fig. 13.

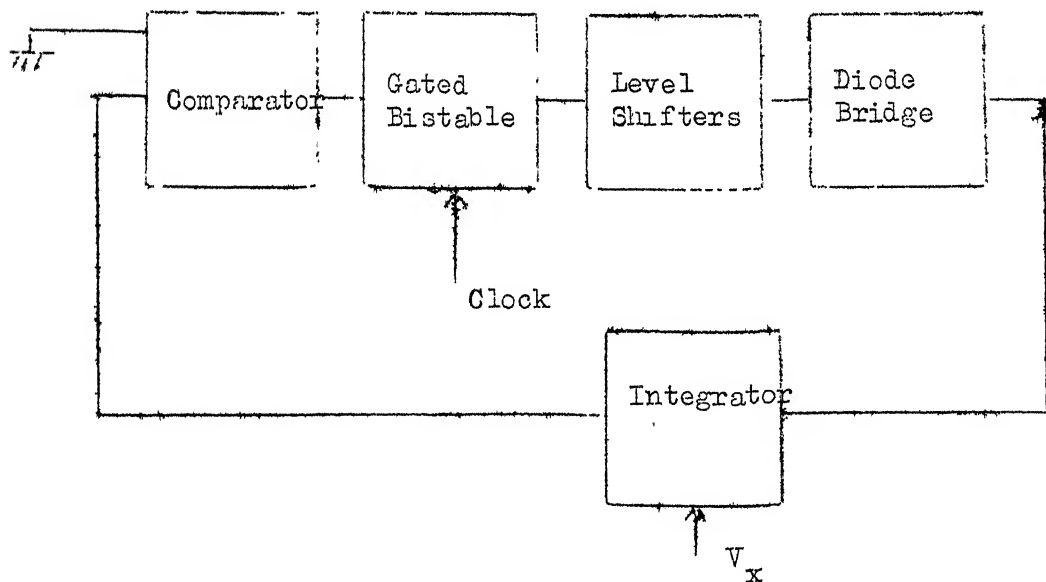


Fig. 13

The feedback action in the circuit of fig. 13 is similar to that described in connection with the fig. 4. Here the difference is that one point of the comparator input is grounded (This is the same point where V_x is connected in fig. 4 so that the feedback action is not disturbed.) So the output of the integrator will now be a

approximation of the zero level. Also since V_x is now connected to the summing point of the integrator the output is contributed to by V_x as well as the delta pulses. However the sum of the component provided by V_x and the component provided by the delta pulses after integration is required to be zero. Therefore,

$$\frac{1}{RC} \int V_x dt + \int \frac{I}{C} \cdot \frac{V_j}{|V_j|} dt = 0 \quad (6.1)$$

I , as before, is the current switched by the diode bridge. Also $\frac{V_j}{|V_j|}$ has the same interpretation as given in section 4.1.

The Resistance 'R' is connected from V_x to the summing point of the integrator.

The equation (6.1) can be rewritten as

$$\frac{V_x}{RC} = - \frac{I}{C} \frac{V_j}{|V_j|}$$

or
$$\frac{V_j}{|V_j|} = - \frac{V_x}{IR} \quad (6.2)$$

So $\frac{V_j}{|V_j|}$, which is the switching function associated with the delta pulses, directly represents V_x instead of dV_x/dt as was the case in the original quantiser.

6.2. Output Voltage in the modified integrator

The multiplier unit in the modified integrator is unchanged. Hence, using the same symbols that were used in Section 4.1,

$$V_z = - \frac{1}{T_m} \int \frac{V_j}{|V_j|} V_y dt.$$

And using equation 6.2,

$$V_z = \frac{1}{T_m I.R} \int V_x V_y dt \quad (6.3)$$

or
$$V_z = K_m \int V_x V_y dt$$

where
$$K_m = \frac{1}{I.R.T_m} \quad (6.4)$$

6.3. The modified integrator used as a multiplier of two analog signals

If the modified integrator is further modified by employing a feedback in the integrator that is associated with the multiplier unit and the time constants are properly adjusted then it can be used as a multiplier of two analog signals. This is shown in Fig. 14.

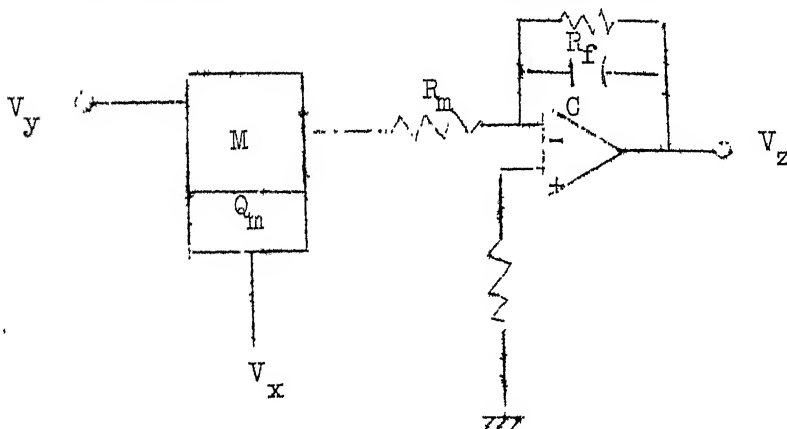


Fig. 14

It can be seen that the normal integrator O_3 of fig. 8 is modified by connecting a feedback resistor R_F across G . Such an integrator has the Bode plot which is shown in Fig. 15.

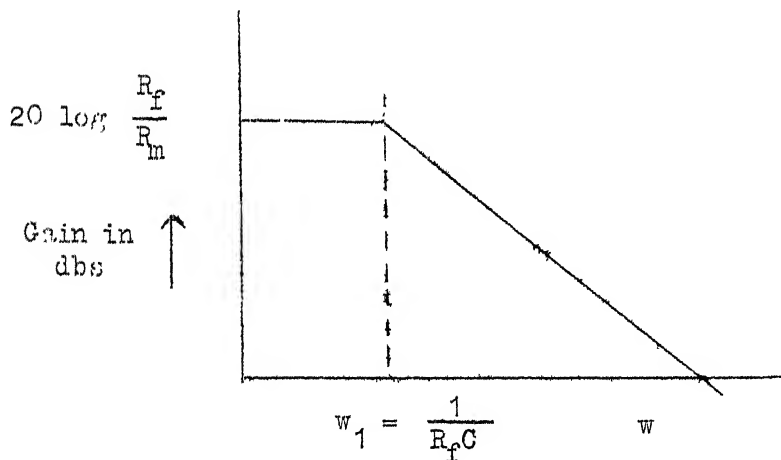


Fig. 15

It can be seen that the break point occurs at $w_1 = \frac{1}{R_F C}$. Therefore if R_F and C are chosen such that w_1 is much more than the signal frequency then the integrator O_1 of Fig. 14 is simply acting as a filter to reduce the switching component in the multiplied signal. Hence the output will represent multiplication of the two signals V_y and V_x within a scale factor.

Since the OP-AMP O_1 of Fig. 14 is now acting as a simple amplifier for the signal frequencies the output voltage can be written as

$$V_z = \frac{R_F}{R_m} \cdot \frac{1}{I \cdot R} V_x \cdot V_y \quad (6.5)$$

I and R are explained in connection with equation (6.1).

As an example, consider

$$V_x = V_y = 4 \sin 2\pi \cdot 30 t.$$

Since the signal frequency is 30 c/s, the OP-AMP C_1 of Fig. 14 will act as an amplifier when the breakpoint shown in Fig. 15 is more than 30 c/s. The break point at 300 c/s will be satisfactory.

Thus if $R_F = 40K\Omega$ to put the d.c. gain at 4 (since $R_m = 10K\Omega$), C is given by the following equation.

$$300 = \frac{1}{2\pi \times 40 \times 10^3 \times C}$$

or $C \approx .04 \mu F$

And $C = .05 \mu F$ will also do the job as it will keep the first break point much above 30 c/s.

If $R = 5 K\Omega$

$$I = 3mA,$$

$$V_{z_{\max}} = 4.26 \text{ Volts.}$$

and

$$V_z = 4.26 \sin^2 2\pi \cdot 30t.$$

6.3* Multiplier used for generating polynomials.

A polynomial in $x(t)$, given by $y = a_0 + a_1x + a_2x^2 + \dots$, can be easily generated as shown in the fig. 15*.

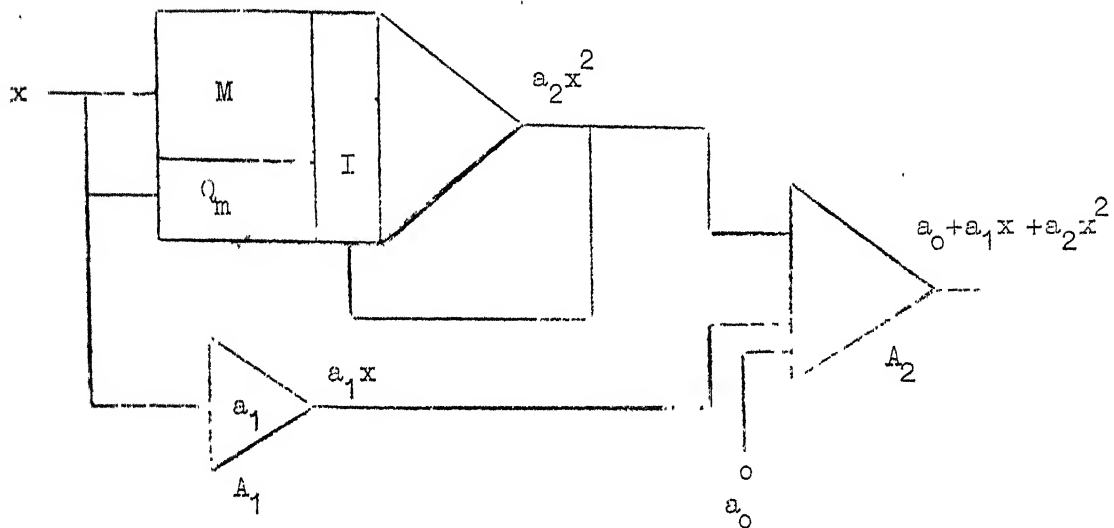


Fig. 15*

In Fig. 15*, the modified integrator is used in the feedback mode so that it operates like a multiplier. The constant of such a multiplier is given by $\frac{R_f}{R_m} \times \frac{1}{I \times R}$ (see equation 6.5). This can be adjusted to a_2 . A_1 is an amplifier with a gain a_1 and A_2 is an adder. By adjusting the constants a_0 , a_1 , a_2 etc., Hermite polynomial of any degree can also be generated.

6.4. Oscillator with Voltage Control of Frequency

With reference to Fig. 12, if quantiser units of both the integrators are operated in the modified mode then a voltage controlled oscillator is obtained. This is explained below.

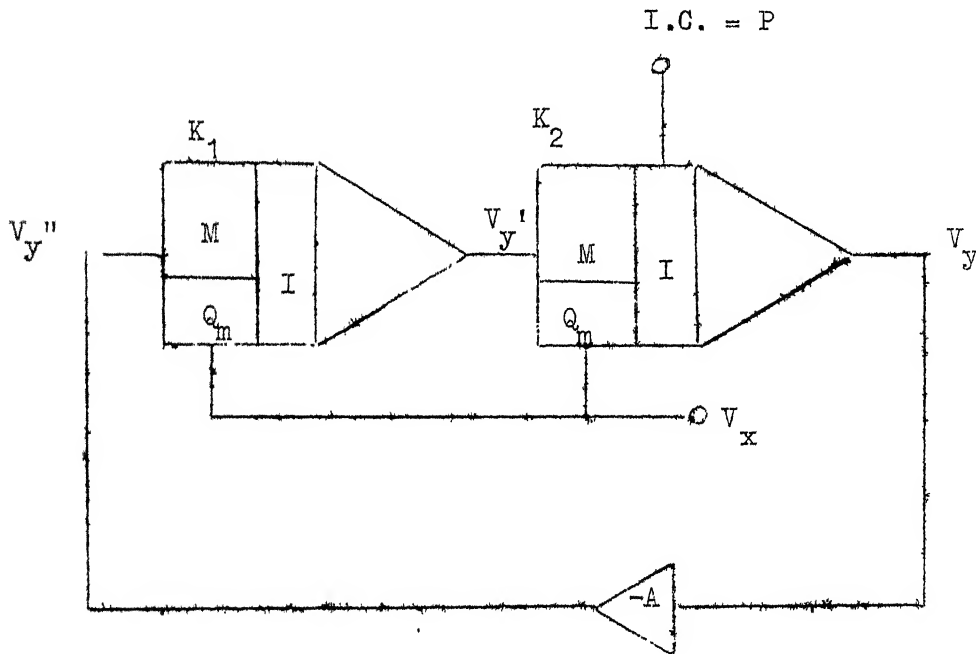


Fig. 17

K_1 and K_2 are the constants given by the equation (6.4).

Now, referring to Fig. 17,

$$V_y'' = -A V_y \quad (6.6)$$

and

$$V_y' = K_1 \int V_y'' V_x dt \quad (6.7)$$

From equations (6.6) and (6.7),

$$V_y' = -AK_1 \int V_y V_x dt \quad (6.8)$$

Also
$$V_y = K_2 \int V_y' V_x dt \quad (6.9)$$

From equations (6.8) and (6.9)

$$V_y = K_2 \int (-AK_1 \int V_y V_x dt) V_x dt.$$

Therefore

$$\frac{dV_y}{dt} = -AK_1 K_2 V_x \int V_y V_x dt$$

or
$$\frac{d^2 V_y}{dt^2} = -AK_1 K_2 V_x^2 V_y \quad (6.10)$$

The solution to the equation (6.10) is

$$V_y = P \cos V_x \sqrt{AK_1 K_2} \cdot t$$

when $V_y = P$ at $t = 0$.

Thus the circuit oscillates at a frequency which is directly proportional to V_x .

As an example if $K_1 = K_2 = K$ and K is given by equation (6.4).

If

$$\begin{aligned} R_m &= 10K\Omega \\ C &= 1 \mu F \\ I &= 3 \text{ mA} \\ R &= 5 K\Omega \end{aligned}$$

$$\therefore K = \frac{100}{15} \quad \frac{1}{V\text{-Sec.}}$$

If $\Lambda = 9$

$$w = \frac{300}{15} V_x \quad \text{rad./sec.}$$

and
$$F = \frac{10}{\pi} V_x \quad \text{c/s.}$$

CHAPTER 7

CONCLUDING REMARKS

7.1. Panel description :-

The panel diagram is shown in the fig. 18. The terminals for connecting C , R , C_m and R_f are brought out as the values of these may have to be different in different applications for proper scaling.

The switch labeled V_- is used for connecting V_- to earth (required for adjusting the slopes in the quantiser) or to F (when the quantiser functions). The potentiometer labeled $I.C.$ sets the desired initial condition voltage. This is calibrated.

The Bandswitch $B.S.1$ is used for putting the integrator in initial condition or compute or in the REP-OP mode. The band-switch $B.S.2$ is used for operating the integrator either in the Normal or the modified mode. The terminals for Op-Amps O_1 and O_2 are brought out so that they can be used in the appropriate fashion for different applications.

7.2. Other Applications:

In its role as an analogue-digital convertor, the modified quantiser may be used to convert an analog signal into delta pulse form, which may be stored in a conventional shift register. This arrangement provides the facility of a function store.

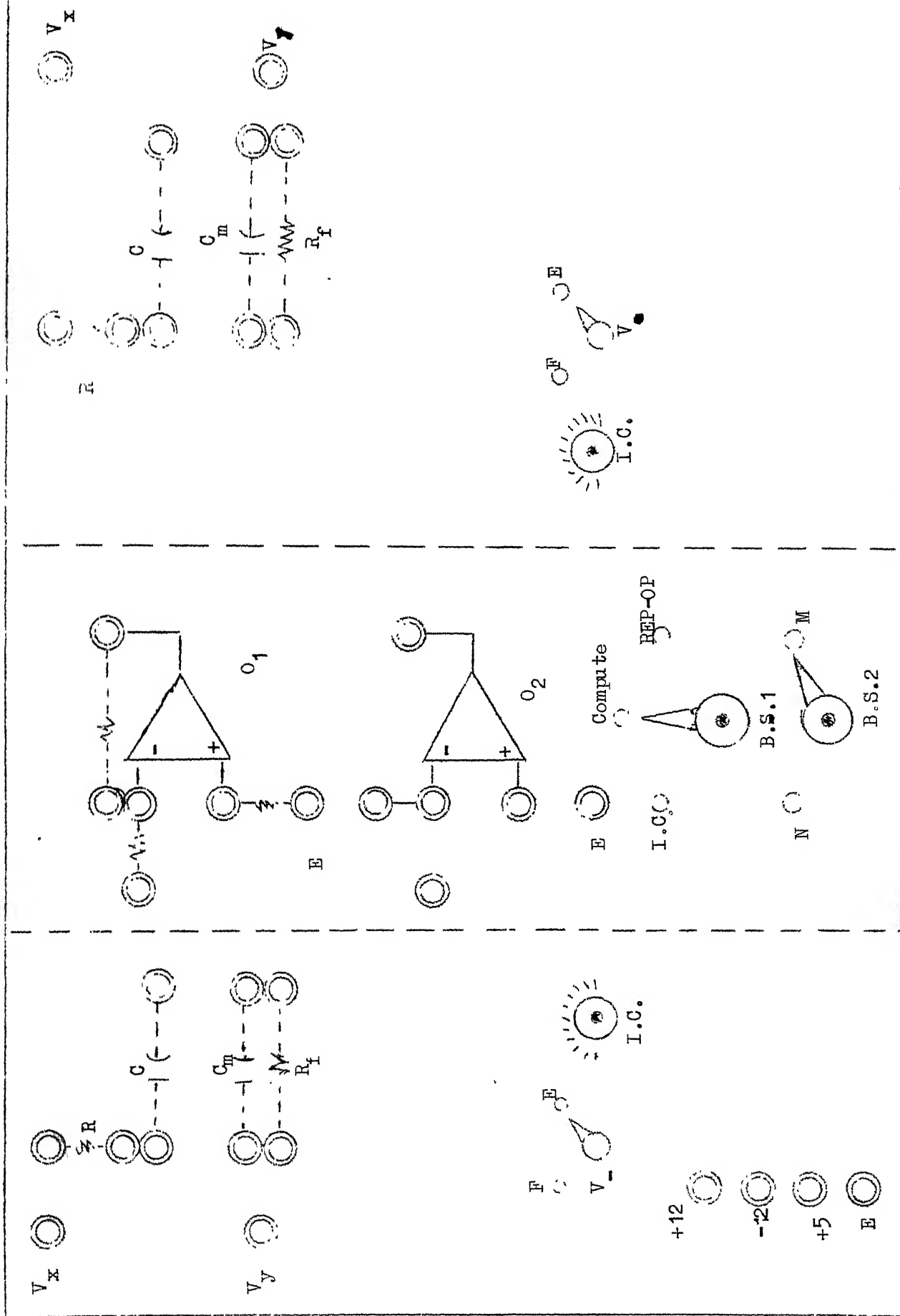


FIGURE 18

Function storage may be used for the iterative solution of integral equations and certain forms of partial differential equations.

7.3. Results:-

Fig. 19 shows the results from the circuit which was set up for generating x^2 from x . The method for this is discussed in section 6.3*. The plot which was obtained by using a strip-chart recorder, shows the input $V_x = 4 \sin 2\pi (.05)t$ and the output $V_z = K_m 16 \sin^2 2\pi (.05)t$, where K_m is the scaling constant and is given by

$$K_m = \frac{R_f}{R_m} \cdot \frac{1}{I.R}$$

The various element values were set as follows.

$$R_f = 10K \Omega; \quad R_f = 10K \Omega (.1\%)$$

$$(.1\%)$$

$$R = 2K \quad (.1\%)$$

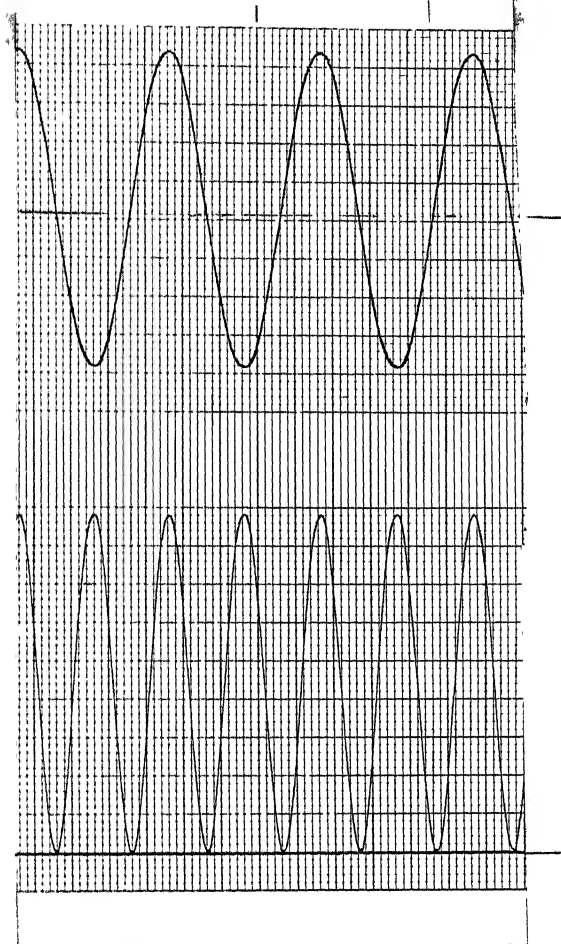
$$\text{Also, since } I/C = 3570 \text{ V/sec. and } C = 1 \mu F (5\%)$$

$$I = 3.57 \text{ mA.}$$

$$\therefore K_m = 1/7.14 \text{ (Volts)}^{-1}$$

So the output V_z should be

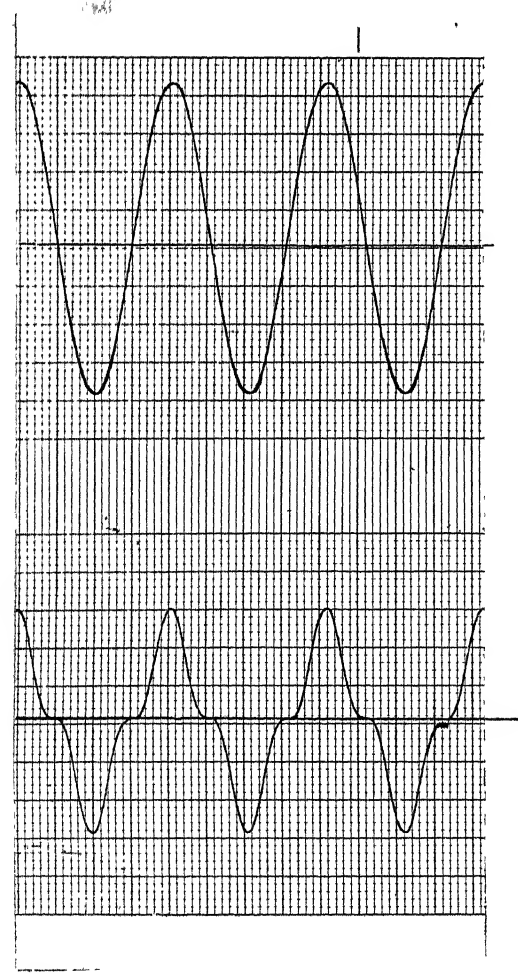
$$V_z = 2.28 \sin^2 2\pi (.05)t.$$



$x(t)$

Fig 19

$x^2(t)$



$x(t)$

Fig. 20

$x^3(t)$

Now for the strip-chart recorder the scales were set as follows.

$$\text{Chart Speed} = 1\text{mm/sec.}$$

$$\text{Vertical scale of } V_x = .2\text{V/mm.}$$

$$\text{Vertical scale of } K_m V_x^2 = .05\text{V/mm.}$$

So the recorded plot is

$$V_z = 2.2 \sin^2 2\pi(.05)t.$$

An error of slightly less than 5%. Fig. 20 shows the plot for x^3 . Here the voltage $V_x = 4 \sin 2\pi(.05)t$ is multiplied with

$$V_y = 2.2 \sin^2 2\pi(.05)t$$

So the output should be

$$V_z = K_m V_x V_y = K_m 8.8 \sin^3 2\pi(.05)t$$

V And K_m , in this case was adjusted to be $1/5.8 \text{ (Volts)}^{-1}$.

So,

$$V_z = 1.51 \sin^3 2\pi(.05)t.$$

In this case scales were set as follows.

$$\text{Chart speed} = 1\text{mm/sec.}$$

$$\text{Vertical scale for } V_x = .2\text{V/mm.}$$

$$\text{Vertical scale of } V_z = .1\text{V/mm.}$$

So from the plot

$$V_z = 1.51 \sin^3 2\pi(.05)t.$$

In the use of the generalised integrator a problem faced is that the OP-AMP O_3 of fig. 8 gradually goes into saturation after the integration is started. This may be because of asymmetry in the FET-sampling-circuit that is employed in the multiplier portion of the generalised integrator. Use of tracking FETs is suggested to remedy this defect. Another possible cause is the drift in the integrator. This can be offset by the addition of an appropriate amount of D. C. voltage to the integrator. This voltage, however, will have to be adjusted from time to time.

REFERENCES

1. Paul and Gatland - "Design and applications of a generalised integrator", Proc. IEE September 1967, Volume 114, No.9
2. Millman and Taub - "Pulse, Digital and switching waveforms", McGraw-Hill.
3. Graeme and Tobey - "Operational Amplifiers - Design and Application", McGraw-Hill.